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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Geoffrey S. Strongin Dale E. Gulick	Examiner: B. Lanier
Serial No.: 09/852,942	Group Art Unit: 2132
Filed: May 10, 2001	Att'y Docket: 2000.038400
For: COMPUTER SYSTEM ARCHITECTURE FOR ENHANCED SECURITY AND MANAGEABILITY	Customer No. 023720

APPEAL BRIEF

CERTIFICATE OF MAILING
37 C.F.R. 1.8

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date below:

11.10.05 (Date) Kathy Jones (Signature)

Commissioner of Patents
P.O. Box 1450
Alexandria, Va 22313-1450

Sir:

Applicant hereby submits this Appeal Brief to the Board of Patent Appeals and Interferences in response to the final Office Action dated June 24, 2005. A Notice of Appeal was filed on September 21, 2005 and so this Appeal Brief is believed to be timely filed.

The Commissioner is authorized to deduct the fee for filing this Appeal Brief ($500) from **Advanced Micro Devices, Inc.'s Deposit No. 01-0365/TT3757.**[1]

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[1] In the event the monies in that account are insufficient, the Director is authorized to withdraw funds from Williams, Morgan & Amerson, P.C. Deposit Account No. 50-0786/2000.038400.

I. REAL PARTY IN INTEREST

The present application is owned by Advanced Micro Devices, Inc. The assignment of the present application to Advanced Micro Devices, Inc., is recorded at Reel 11808, Frame 0806.

II. RELATED APPEALS AND INTERFERENCES

Applicant is not aware of any related appeals and/or interferences that might affect the outcome of this proceeding.

III. STATUS OF THE CLAIMS

Claims 1-29 are pending in the application. Claims 1-4, 10-16, 18-20, 23-26, and 28-29 stand rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Chang, et al. (U.S. Patent No. 6,286,097). Claims 5-9, 17, 21-22, and 27 stand rejected under 35 U.S.C. 103(a) as allegedly being obvious over Chang in view of Davis (U.S. Patent No. 5,844,986).

IV. STATUS OF AMENDMENTS

There were no amendments after the final rejections.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Claims 1, 14, 20, 23, and 24 set forth a processor, a device coupled to the processor, and a memory selectably coupled to the device and the processor. Claims 1, 14, 20, 23, and 24 also set forth a switching mechanism coupled between the memory and each of the processor and the device, wherein the switching mechanism includes a first state providing access from the

processor to the memory and a second state providing access from the device to the memory. In claim 1, the device is a bridge.

For example, Figs. 19A, 19B, and 19C illustrate block diagrams of embodiments 3000A, 3000B, and 3000C of computer systems with a BIOS ROM 355 accessible to the processor 805 at boot time and to the south bridge 330 at other times. Common to all three figures are a processor 805, a south bridge 330, control logic 3010, a boot switch 3005, a crypto-processor 305, and BIOS ROM 355. The processor 805 is coupled to the south bridge 330 in a usual fashion at times other than at boot time. At boot time, the control logic 3010 is operable to change the boot switch 3005 such that the processor 805 has access to the BIOS 355 without going through the south bridge 330 in the usual fashion. See Patent Application, page 60, ll. 1-8.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Appellant respectfully requests that the Board review and overturn the two rejections present in this case. The following issues are presented on appeal in this case:

(A) Whether claims 1-4, 10-16, 18-20, 23-26, and 28-29 are anticipated by Chang;

(B) Whether claims 5-9, 17, 21-22, and 27 are obvious over Chang in view of Davis.

VII. ARGUMENT

A. Legal Standards

An anticipating reference by definition must disclose every limitation of the rejected claim in the same relationship to one another as set forth in the claim. *In re Bond*, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990).

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. That is, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. Third, there must be a reasonable expectation of success.

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. A recent Federal Circuit case emphasizes that, in an obviousness situation, the prior art must disclose each and every element of the claimed invention, and that any motivation to combine or modify the prior art must be based upon a suggestion in the prior art. *In re Lee*, 61 U.S.P.Q.2d 143 (Fed. Cir. 2002). Conclusory statements regarding common knowledge and common sense are insufficient to support a finding of obviousness. *Id.* at 1434-35. Moreover, it is the claimed invention, as a whole, that must be considered for purposes of determining obviousness. A mere selection of various bits and pieces of the claimed invention from various sources of prior art

does not render a claimed invention obvious, unless there is a suggestion or motivation in the prior art for the claimed invention, when considered as a whole.

It is by now well established that teaching away by the prior art constitutes *prima facie* evidence that the claimed invention is not obvious. *See, inter alia, In re Fine,* 5 U.S.P.Q.2d (BNA) 1596, 1599 (Fed. Cir. 1988); *In re Nielson*, 2 U.S.P.Q.2d (BNA) 1525, 1528 (Fed. Cir. 1987); *In re Hedges*, 228 U.S.P.Q. (BNA) 685, 687 (Fed. Cir. 1986).

B. Claims 1-4, 10-16, 18-20, 23-26, and 28-29 are not anticipated by Chang.

Chang describes a computer chipset 320 that is coupled to a main processor 310, a peripheral device 340, and a Read Only Memory (ROM) 350. The main processor 310 is coupled to a main control circuit 321 on the chipset 320. The main control circuit 321 is coupled to a peripheral control circuit 322 and a booting control circuit 323. The peripheral control circuit 322 and the booting control circuit 323 provide inputs A and B, respectively, to a switching circuit 325, which provides one of the inputs A or B as an output Y to the peripheral device 340 or the ROM 350 based upon a booting enable signal (BTEN) provided to an input/output port S of the switching circuit 325 by the booting control circuit 323. When the booting enable signal (BTEN) is activated, the switching circuit 325 connects the booting control circuit 323 to the ROM 350. Contents of the ROM 350 may then be moved to the main memory 330. When the booting enable signal (BTEN) is not activated, the switching circuit 325 connects the peripheral control circuit 322 to the peripheral device 340. See Chang, col. 7, ll. 43-62 and Figure 8.

Applicants submit that the computer system 300 described above permits switching between two alternate and parallel circuits. The first circuit couples the main memory 330 to the

booting control circuit 323, which is then connected to the ROM 350. The second circuit couples the peripheral control unit 322 to the peripheral device 340. However, Applicants respectfully submit that Chang does not describe or suggest a switching mechanism that provides a first state providing access from a processor to a memory and a second state providing access from the device to the memory, *i.e.*, the second state permits the device to access the same memory as the processor has access to in the first state.

For at least the aforementioned reasons, Applicants respectfully submit that the present invention is not anticipated by Chang and request that the Examiner's rejections of claims 1-4, 10-16, 18-20, 23-26, and 28-29 under 35 U.S.C. 102(e) be REVERSED.

C. Claims 5-9, 17, 21-22, and 27 are not obvious over Chang in view of Davis.

As discussed above, Chang fails to teach or suggest a switching mechanism that provides a first state providing access from a processor to a memory and a second state providing access from the device to the memory, as set forth in independent claims 1, 14, 20, 23, and 24. The Examiner relies upon Davis to describe a secure BIOS ROM housed within a crypto-processor. Davis does not, however, remedy the fundamental deficiencies in Chang. Thus, Applicants respectfully submit that the prior art of record fails to teach or suggest all the limitations of the claimed invention.

Applicants also respectfully submit that the cited references fail to provide any suggestion or motivation to modify the prior art of record to arrive at the claimed invention. To the contrary, Chang teaches away from the claimed invention. In particular, Chang describes two alternate and parallel circuits. The first circuit couples the main memory 330 to the booting control circuit 323, which is then connected to the ROM 350. The second circuit couples the

peripheral control unit 322 to the peripheral device 340. Thus, Applicants respectfully submit that Chang teaches away from a switching mechanism that provides a first state providing access from a processor to a memory and a second state providing access from the device to the memory, *i.e.*, the second state permits the device to access the same memory as the processor has access to in the first state.

For at least the aforementioned reasons, Applicants respectfully submit that the Examiner has failed to make a *prima facie* case that the present invention is obvious over Chang in view of Davis. Applicants respectfully request that the Examiner's rejections of claims 5-9, 17, 21-22, and 27 under 35 U.S.C. 103(a) be REVERSED.

VIII. CLAIMS APPENDIX

The claims that are the subject of the present appeal – claims 1-29 – are set forth in the attached "Claims Appendix."

IX. EVIDENCE APPENDIX

There is no separate Evidence Appendix for this appeal.

X. RELATED PROCEEDINGS APPENDIX

There is no Related Proceedings Appendix for this appeal.

XI. CONCLUSION

In view of the foregoing, it is respectfully submitted that the Examiner erred in not allowing all claims pending in the present application, claims 1-29, over the prior art of record.

The undersigned may be contacted at (713) 934-4052 with respect to any questions, comments or suggestions relating to this appeal.

Respectfully submitted,

Date: 11/10/05

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AGENT FOR APPLICANTS

CLAIMS APPENDIX

1. (Original) A system, comprising:

a processor;

a bridge coupled to the processor;

a memory selectably coupled to the bridge and the processor; and

a switching mechanism coupled between the memory and each of the processor and the bridge, wherein the switching mechanism includes a first state providing access from the processor to the memory and a second state providing access from the bridge to the memory.

2. (Original) The system of claim 1, further comprising:

control logic coupled to the switching mechanism for controlling changes between the first state and the second state.

3. (Original) The system of claim 2, further comprising:

a second bridge coupled between the bridge and the processor, wherein the control logic is comprised within or controlled by the second bridge.

4. (Original) The system of claim 2, wherein the control logic is comprised within or controlled by the processor.

5. (Original) The system of claim 2, further comprising:

a crypto-processor coupled to the memory, wherein accesses to the memory pass through the crypto-processor.

6. (Original) The system of claim 5, wherein the control logic is comprised within or controlled by the crypto-processor.

7. (Original) The system of claim 1, further comprising:

a crypto-processor coupled to the memory, wherein accesses to the memory pass through the crypto-processor.

8. (Original) The system of claim 7, wherein the crypto-processor is further coupled to the switching mechanism; and wherein the switching mechanism couples the crypto-processor to the processor in the first state and to the bridge in the second state.

9. (Original) The system of claim 5, further comprising:

a local bus;

a first I/O bus;

a second I/O bus; and

a second bridge coupled between the bridge and the processor, wherein the second bridge is coupled to the processor through the local bus, and wherein the second bridge is coupled to the bridge through the first I/O bus; and

wherein the crypto-processor is coupled to the processor through the local bus in the first state, and wherein the crypto-processor is coupled to the bridge through the second I/O bus in the second state.

10. (Original) The system of claim 1, wherein the memory and the bridge are coupled to an I/O bus; wherein the bridge further comprises I/O bus interface logic for communicating on the I/O bus; wherein the processor further comprises I/O bus interface logic for communicating on the I/O bus; wherein the switching mechanism is coupled to the I/O bus; wherein the processor is coupled to the switching mechanism through the I/O bus interface logic; wherein the first state comprises the I/O bus interface logic of the processor being configured to communicate with the memory over the I/O bus, and wherein the second state comprises the I/O bus interface logic of the bridge being configured to communicate with the memory over the I/O bus.

11. (Previously Presented) The system of claim 9, wherein the second I/O bus comprises an LPC bus.

12. (Original) The system of claim 1, wherein the memory is a ROM or flash memory.

13. (Original) The system of claim 12, wherein the ROM or the flash memory includes a BIOS ROM.

14. (Original) A method for operating a computer system comprising a processor, a memory, and a first device, wherein the processor is operably coupled to the first device, and the first device is operably coupled to the memory, the method comprising:

coupling the processor and the memory using a switching mechanism, wherein the switching mechanism is configured to operate in a first state operably coupling the first device to the memory and a second state operably coupling the processor to the memory;

switching the computer system into the second state, thereby operably coupling the memory to the processor using the switching mechanism; and

reading from the memory in the second state.

15. (Original) The method of claim 14, wherein the processor is coupled to the first device through at least a system bus, wherein the first device is coupled to the memory through a first I/O bus, wherein coupling the processor and the memory using the switching mechanism comprises coupling the processor to the first I/O bus through the switching mechanism.

16. (Original) The method of claim 14, wherein the second state comprises booting the computer system, wherein the memory comprises a ROM, and wherein reading from the memory comprises reading BIOS information from the ROM.

17. (Original) The method of claim 14, wherein the memory comprises secure storage, wherein the second state comprises reading from the secure storage, and wherein reading from the memory comprises reading secure data from the secure storage.

18. (Original) The method of claim 14, further comprising:

switching the computer system into the first state.

19. (Original) The method of claim 18, further comprising:

reading from the memory in the first state.

20. (Original) A computer system comprising:

a processor;

a memory;

a first device operably coupled to the processor and to the memory;

means for switching between a first state where the first device is operably coupled to the memory and a second state where the processor is operably coupled to the memory; and

means for controlling the means for switching.

21. (Original) The computer system of claim 20, further comprising:

a crypto-processor coupled to the memory, wherein accesses to the memory pass through the crypto-processor.

22. (Original) The system of claim 21, wherein the crypto-processor is further coupled to the switching mechanism; and wherein the switching mechanism couples the crypto-processor to the processor in the first state and to the bridge in the second state.

23. (Original) A computer system, comprising:

means for switching the computer system from a first state to a second state, thereby operably coupling a memory to a processor in the second state;

means for coupling the processor and the memory using the means for switching, wherein the means for switching is configured to place the computer system in a first state operably coupling the a device to the memory and in a second state operably coupling the processor to the memory;

means for reading from the memory in the second state; and

means for reading from the memory in the first state.

24. (Original) A computer readable program storage device encoded with instructions that, when executed by a computer system comprising a processor, a memory, and a first device, wherein the processor is operably coupled to the first device, and the first device is operably coupled to the memory, performs a method of operating the computer system, the method comprising:

coupling the processor and the memory using a switching mechanism, wherein the switching mechanism is configured to operate in a first state operably coupling the first device to the memory and a second state operably coupling the processor to the memory;

switching the computer system into the second state, thereby operably coupling the memory to the processor using the switching mechanism; and

reading from the memory in the second state.

25. (Original) The computer readable program storage device of claim 24, wherein the processor is coupled to the first device through at least a system bus, wherein the first device is coupled to the memory through a first I/O bus, wherein coupling the processor and the memory using the switching mechanism comprises coupling the processor to the first I/O bus through the switching mechanism.

26. (Original) The computer readable program storage device of claim 24, wherein the second state comprises booting the computer system, wherein the memory comprises a ROM, and wherein reading from the memory comprises reading BIOS information from the ROM.

27. (Original) The computer readable program storage device of claim 24, wherein the memory comprises secure storage, wherein the second state comprises reading from the secure storage, and wherein reading from the memory comprises reading secure data from the secure storage.

28. (Original) The computer readable program storage device of claim 24, the method further comprising:

switching the computer system into the first state.

29. (Original) The computer readable program storage device of claim 28, the method further comprising:

reading from the memory in the first state.